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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,989	10/17/2000	Yoshitaka TSUNASHIMA	04329.1952-01000	2408

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/688,989	TSUNASHIMA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/05/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27,28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *27,28 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on November 17, 006 has been entered and forwarded to the examiner on December 05, 2006.

Therefore claim 27 as amended by the amendment and claims 28 and 3034 as previously recited are currently pending in the Application.

Claim Rejections. 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action : (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27-28 and 30 to 34 rejected under 35 U.S.C. 103(a) as being unpatentable over De LA Moneda et al. (U.S. Patent No. 4,45, 267, herein after De La Moneda, previously applied) and further in view of AAPR (Applicants' Admitted Prior Art shown at least in figs. 1- 3F and describe~ in the specification at page 6 lines 1-17 etc.).

With respect to claim 27 De La Moneda describes a semiconductor device comprising: a semiconductor substrate including a first and second region separated by an isolation element, (De La Moneda figs. 1-1 # lo-substrate, figs. #12 isolation

element col. 4 lines 20-25 etc.) a first transistor formed on the first region of the substrate (claim 7, col. 6 lines 35-40) and including a first insulation film (figs. # 16, and including a second insulation film and a second gate electrode arranged along the first direction, (figs. Structure above 18) wherein a first side wall is located at an end of the first gate electrode in the first direction, a second side wall is located at an end of the second gate electrode in the first direction, and the first side wall is directly physically and without the presence of additional layers there between connected to the second side wall above the isolation element when viewed from a direction perpendicular to the first direction. (fig 10 # 42 connecting over isolation element 12).

De La Moneda does not specifically mention the presently newly added limitation of "the sidewall of the first gate electrode is directly physically and with out the presence of additional layers there between" However AAPR in at least figures 1 to 3 E and the description in page 6 lines 1-17 shows and describes both physical and electrical direct connection between element 16 and first and second gates including their sidewalls to provide a method that uses conventional processing steps to form a junction between adjacent electrodes. This in turn saves valuable real estate by reducing number on inter level connections required and thus uses less number of steps to form the device.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include AAPR's the sidewall of the first gate electrode is directly physically and with out the presence of additional layers there between In De La Moneda' s device. The motivation to make the above combination (as is known to one of ordinary skill in the art) is to provide a method that uses conventional processing

steps to form a junction between adjacent electrodes. This in turn saves valuable real estate by reducing number on inter level connections required and thus uses less number of steps to form the device.

With respect to claim 28, De La Moneda describes a device according to claim 33, wherein a side of the side insulator film is on a surface of said semiconductor. (De La Moneda figures e.g. fig. 10 #38, col. 12-16).

With respect to claim 30 De La Moneda describes a device according to claim 28, wherein at least one of said first and second gate electrodes is formed by a damascene gate process.. (De La Moneda figures 1-11 , same as Applicants' description at least at page 9 lines 10-25 and page 26 lines 2 to 20 for their gate formation).

With respect to claim 31 De La Moneda describes a device according to claim 33, wherein said first insulation film is thinner than said second insulation film, said first transistor forms a logic circuit, and said second transistor forms a memory cell. (De La Moneda figures, col.2 lines 30-36).

With respect to claim 32 De La Moneda describes a device according to claim 33, wherein top surfaces of said first and second gate electrodes are coplanar. (De La Moneda figures).

With respect to claim 33 De La Moneda describes a device according to claim 27, wherein said second transistor further comprises a polysilicon layer formed on the second insulation film formed on the substrate, (De La Moneda figure 10 # 20 over 16) and a side insulator film formed en a side of the second insulation film and a side wall of

the polysilicon layer, (De La Moneda figure 10 # 38) said second gate electrode is formed on the polysilicon layer, (De La Moneda figure 10) and connected to the side wall of the second insulation film and the side wall of the polysilicon layer via the side insulator film substrate. (De La Moneda figures specifically 10 and col. 6.,7).

With respect to claim 34 De La Modena describes a device to claim 27, wherein the side wall of the first gate electrode is directly connected to the side wall of the second gate electrode. (De La Modena figure 10 and see also Applicants' admitted prior art at least in figures 1-3E and the description at least page 6 lines 1-17 (especially 9-17).

Response to Arguments

Applicant's arguments filed 12/05/2006 have been fully considered but they are not persuasive for the following reasons :

Applicants' argument regarding the applied De La Moneda reference repeats what was stated in the Office's rejection and need not be addressed further.

Applicants' contention with regard to AAPR (Applicants' Admitted Prior Art) that , "Fig. 3E of Applicants' specification shows a second gate electrode 15 is connected to a tungsten silicide film 16. However, a side wall located at the end of the second gate electrode 15 is not connected to a side wall at the end of the tungsten silicide film 16. Instead, the side wall at the end of the second gate electrode 15 is connected to a mid-portion of the tungsten silicide film 16 . Therefore, Fig. 3E fails to teach the claimed "first side wall is located at an end of the first gate electrode in the first direction, a second side wall is located at an end of the second gate electrode in the first direction, and the

first side wall is directly physically and without the presence of additional layers there between connected to the second side wall above the isolation element," as recited in amended claim 27 ", is not persuasive because Applicants' above interpretation is not an incomplete reading of the applied reference for the following reasons :

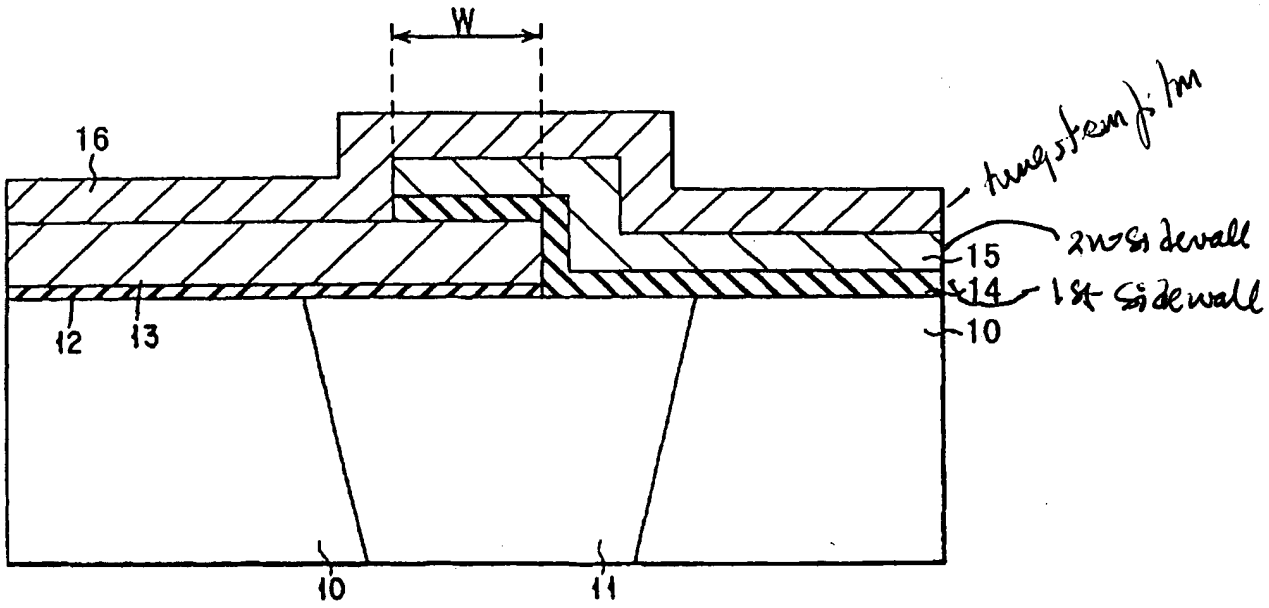

FIG. 3E (PRIOR ART)

In Fig. 3E , Applicants' are correct in identifying elements 14 and 15 as the first and second gates .

However Applicants' must (as per their presently recited claims) must identify the first side wall is located at an end of the first gate electrode in the first direction as the side wall of 14 (at the right extreme of 14 when looking at it).

Similarly Applicants' must (as per their presently recited claims) must identify identify a second side wall is located at an end of the second gate electrode in the first

direction as the sidewall of 15 above sidewall of 14 (at the right extreme of 15 when looking at it) and further to meet the recitation located at an end of the second gate electrode and in the first direction (emphasis supplied) which is (and the first side wall) directly physically and without the presence of additional layers there between connected to the second side wall above the isolation element. (all of which are above isolation element 12e.g. fig. 3E).

Applicants' equating the other end of gate electrode 15 and the corresponding sidewall at that end as the one is not commensurate with the presently recited claims and further based on this assumption concluding this side wall of 15 (at the other end) is connected to the mid-portion of the tungsten silicide film 16 (which is further processed to form third electrode) cannot form the basis of an convincing argument .

Therefore all of Applicants' arguments are not persuasive and all pending claims are finally rejected.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven H. Rao

Patent Examiner

February 05, 2007.

HOWARD WEISS
PRIMARY EXAMINER